Multi-Scale Simulation for CPI Stress Induced Carrier Mobility Shift in Advanced Si Nodes


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Outline

- Introduction
- Multi-scale Simulation Approach
- CPI Stress Distribution in Planar and FinFET
- Experimental Measurements
- Performance Map
- Package Structure Study & Verification
- Conclusions
Performance Shift

*Die-Package Stress Interaction Impact on Transistor Performance*

by Leatherman et al. (IRPS, IEEE 2012)

Ring Oscillator measurement:

- 6% frequency shift due to CPI stress
To manage e-CPI risk, it needs the collaboration of entire semiconductor industry

- Circuit designers
- Package designers
- Silicon foundries
- Package assembly houses
Where to put the device?

- Mobility and transistor performance are never uniform throughout a die under packaging stress.
- Max stress gradient is about 1MPa per um.
- Difference of mobility change can be larger than 10% to 30% under packaging stress.
Performance Shift under CPI Stress

- Piezoresistance model to simulate mobility shift

\[ \frac{\Delta I_D}{I_D} = \frac{\Delta \mu}{\mu} = \pi \sigma = \pi_x \sigma_x + \pi_y \sigma_y + \pi_z \sigma_z \]

where \( \sigma = \sigma_{\text{process}} + \sigma_{\text{package}} \)

\[ \frac{\Delta I_D}{I_D} = \frac{\Delta \mu}{\mu} = \pi' \sigma' = \pi_x' \sigma_x' + \pi_y' \sigma_y' + \pi_z' \sigma_z' \]

where \( \sigma' = \text{nominal stress (stress on bulk Si)} \)

- Experiment to measure piezoresistance coefficients vs. stress
  4-point bending for x and y direction
  Cu Bump shear test for z direction

- The measured coefficients are different for devices with different technology, process and design.
Multi-scale Simulation Approach

Global Model in Abaqus
100 mm³ (10¹¹ um³)

Package Model
Stress Distribution in Silicon

1. Construct the global model to simulate the packaging devices

Local Model in Synopsys Sentaurus Interconnect
1 um³ – 10 um³

Stress → Mobility Shift
Piezoresistance Model

2. Import global boundary condition from Abaqus

3. Detailed device from Sentaurus Process

4. Simulate stress effect on device performance

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Han-Ping Pu
CPI Stress Redistribution in Planar MOSFETs

- A FEM model is used to study stress distribution on Planar structure.
- 4-point bending applies compression stress on top surface of silicon substrate (Channel direction $\sigma_x'$ and Width direction $\sigma_y'$).
- $\sigma_x$ and $\sigma_y$ are $\approx 0.9x$ of CPI stress in Channel and Width direction
CPI Stress Redistribution in FinFET ($\sigma_{x'}$)

- A FEM model is used to study stress distribution on Fin structure.
- 4-point bending applies compression stress on top surface of silicon substrate (Channel direction, $\sigma_{x'}$).
- $\sigma_x$ is $\sim 0.7x$ of CPI stress in Channel dir.
CPI Stress Redistribution in FinFET ($\sigma_y'$)

- A FEM model is used to study stress distribution on Fin structure.
- 4-point bending applies compression stress on top surface of silicon substrate (Width direction, $\sigma_y'$).
- $\sigma_y$ is ~3x of CPI stress in Width dir.

![Diagram of FinFET structure with stress redistribution](image.png)
CPI Stress Redistribution in FinFET ($\sigma_z'$)

- A FEM model is used to study stress distribution on Fin structure.
- Bump Shear Test apply vertical stress on top surface of silicon substrate (Vertical direction, $\sigma_z'$).
- $\sigma_z$ is $\sim0.8x$ of CPI stress in Vertical dir.
Experimental Measurements

4-point Bending for stress in X and Y direction

Bump Shear Test for Z direction stress
FinFET vs Planar MOSFET Mobility Shift

- FinFET PMOS shows less shift than Planar
- FinFET NMOS shows comparable shift to Planar

### Measured and Predicted Mobility Shift for FinFET and Planar MOSFETs bending in Channel Direction
### FinFET vs Planar MOSFET Mobility Shift

- FinFET PMOS shows less shift than Planar
- FinFET NMOS shows less shift than Planar

<table>
<thead>
<tr>
<th>Node</th>
<th>Planar</th>
<th>FinFET</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device</td>
<td>p-type</td>
<td>n-type</td>
</tr>
<tr>
<td>$\pi_x'$</td>
<td>- - -</td>
<td>+ + +</td>
</tr>
<tr>
<td>$\pi_y'$</td>
<td>+ + +</td>
<td>+</td>
</tr>
<tr>
<td>$\pi_z'$</td>
<td>+ +</td>
<td>- -</td>
</tr>
</tbody>
</table>

Measured and Predicted shear force / distance match each other in the bump shear test
CPI stress can be calculated using Finite Element Simulation

- If UF is applied, thinner die can increase stress.
- If UF is not applied, thicker die can increase stress.

Stress Contour - Application of Mobility Simulation

![Stress Maps](image-url)

**Stress Map (σₓ’)**

**Stress Map (σｚ’)**

**WLCSP 14 mil**
- with UF
- without UF

**WLCSP 10 mil**
- with UF
- without UF
Performance Map - Application of Mobility Simulation

- This “Performance Map” is based on mobility change due to packaging stress.
- Designers can check the map and find the best location to put the devices.

Performance Map
P-type Core Transistor

Performance Map
N-type Core Transistor
Package Structure Study & Verification

- Package TV: FinFET
- Reliability Test: Pass FT0 and TCB1000
- **N-dominated Ring Oscillator** in T1 area is measured

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<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Technology</strong></td>
<td>FinFET</td>
</tr>
<tr>
<td><strong>Package Form</strong></td>
<td>BGA</td>
</tr>
<tr>
<td><strong>Die Size</strong></td>
<td>7.7 x 8.8 mm²</td>
</tr>
<tr>
<td><strong>Die Thickness</strong></td>
<td>31, 12 mil</td>
</tr>
<tr>
<td><strong>C4 Bump Type</strong></td>
<td>Cu bump</td>
</tr>
<tr>
<td><strong>T1 Area Stress</strong></td>
<td>Compressive (σₓ~σᵧ)</td>
</tr>
<tr>
<td><strong>Test Results</strong></td>
<td>FT0: Pass TCB 1000: Pass</td>
</tr>
</tbody>
</table>

Stress Contour @ 25°C
Si THK = 12 mil

σₓ′  σᵧ′  σ𝒛′
Simulation shows compressive stress ($\sigma_x \sim \sigma_y$) in T1 area

- Piezo-resistance model predicts slow down for NMOS
- Thicker die $\rightarrow$ Smaller stress $\rightarrow$ Less shift

Measured ring oscillator slow down matches prediction

<table>
<thead>
<tr>
<th>FinFET</th>
<th>Stress Condition</th>
<th>Die Thickness</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Units</td>
<td></td>
<td>31 mil</td>
</tr>
<tr>
<td>FT0 result T1 Ring Oscillator</td>
<td>Condition B -55°C ~ +125°C</td>
<td>45 ea</td>
</tr>
<tr>
<td>Slow down 0.2%</td>
<td>Slow down 0.3%</td>
<td></td>
</tr>
<tr>
<td>TC1000 FT result T1 Ring Oscillator</td>
<td>-55°C ~ +125°C</td>
<td>Slow down 0.2%</td>
</tr>
<tr>
<td>Slow down 0.2%</td>
<td>Slow down 0.3%</td>
<td></td>
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</tbody>
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NMOS Mobility Shift (%)
Conclusions

- A multi-scale simulation includes Package finite element model (global) and TCAD (local) is proposed to address e-CPI challenges.
- FinFET has better tolerance regarding to performance shift under CPI stress compared to Planar transistor.
- Performance Map can be a useful tool for designers to manage e-CPI risk.
Thank you!