TCAD Approach for the Assessment of Interconnect Reliability

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Overview

- Full-physical modelling TCAD
- Compact modeling
- Case study I: electromigration in solder bumps
- Case study II: electromigration in through silicon via
- New challenges: Reliability TCAD for nanointerconnects
- Conclusion and outlook
Full-Physics Models of Electromigration

- Material transport for arbitrary 3D layouts
  - Point defect dynamics
  - Mechanical stress
- Grain boundaries and Interfaces
  - Fast diffusivity paths
  - Point defect recombination
Usual approach: Fitting of Black’s equation and time extrapolation

Problems
- Black has derived his equation for straight aluminum interconnect
- Parameters are applicable only for the structures already used for fitting

Full-physics models (Sarychev et al. JAP 1999)
- Applicable to arbitrarily 3D geometries, layouts, and materials
- Extendable with submodels for microstructure and interfaces
- Design of compact model tailored for specific application
- Explanation of different impact factors (geometry, microstructure)

The goal: Through combination of experiments, full physics and compact modeling to design and optimize for reliability
- Multilevel interconnect structures
- Through silicon vias
- Solder bumps
- Nanointerconnects (+ alternative metals)
Electromigration: Time to Failure (TTF)

\[ \frac{\Delta R}{R_0} (\%) \]

\[ \text{Time (a.u.)} \]

Void Initiation

Void Evolution
Electromigration: Void Initiation

\[ t_I \sim \frac{1}{j^2} \]

Simulation Start

→ Electro-Thermal Model

→ Vacancy Dynamics Model

→ Solid Mechanics Model

\[ \text{N} \]

Void is Nucleated?

\[ \text{Y} \]

Ceric et al., IEEE TDMR, vol. 9, 2009,
Electromigration: Void Nucleation

\[ t_N \sim \frac{1}{j} \]

Fridline and Bower, JAP, vol. 85, 1999
Ceric et al., IEICE Tran. Elect. vol 86, 2003,
Lacerda de Orio, PhD thesis, TU Wien, 2005
Compact Modeling

- Compact Modeling
  - Void initiation phase ($t_I$)
  - Void evolution phase ($t_E$)
- Time to failure (TTF)

  \[ TTF = t_I + t_E \]

- Black’s equation
  - A good basis for development
  - Rigorous derivation*

- Full-physics models available
  - Ceric-Orio
  - Sukharev
  - Weide-Zaage

*Shatzkes and Lloyd, JAP, vol. 59, 1986
Case Study: 3D Integration components

- Wafers
- Through Silicon Via (TSV)
- Solder Bump
Solder bump provides electrical connectivity between different functional dies.

Desirable properties: low melting point, mechanical stability, resistance to EM.

Used materials: lead, tin alloys.

Under bump metallization (UBM) is used to reduce effect of current crowding.
Case Study: Solder Bump

Current density ($\times 10^3$ A/cm²)

Ceric et al., SISPAD 2015
Institute for Microelectronics
Case Study: Solder Bump

- Observation from simulation

- Modifying Black’s equation

\[ \sigma \sim j R^2 \sqrt{t} \]

\[ t_f = \left( \frac{A}{j^2} \left( \frac{\sigma_c}{\alpha R^2 + \beta} \right)^2 + \frac{B}{j} \right) \exp \left( \frac{E_a}{kT} \right) \]
Case Study: Solder Bump

![Graph showing the relationship between Log (Time) and Current density (x10^3 A/cm^2) for different values of 2R: 50 sim., 70 sim., 90 sim., 50 eq., 70 eq., 90 eq.](image)
Case Study: Through Silicon Via (TSV)

Test conditions:
- $T = 200^\circ C$
- $J_0 = 1 MA/cm^2$

Boundary conditions:
- Thermal insulation
- Fixed constraints
- Electrical insulation
- EM blocking Cu/TiN

Rovitto et al. ECTC 2016, Rovitto et al. to be submitted Microel. Real.
Case Study: Through Silicon Via (TSV)
Case Study: Through Silicon Via (TSV)

\[
TTF = A J^{-n} \exp\left(\frac{E_a}{k_B T}\right)
\]

\[n = 1.51 \pm 0.05\]
New challenges: Reliability TCAD for Nanointerconnects

- Building a compact model for nanointerconnects (100nn -> 10nm)
- EM is related to resistivity on the atomistic level
  - Both rise due to electron scattering effects
- *Ab initio* relationship between effective “wind” valence $Z_{\text{wind}}(T)$ and resistivity $\rho(T)$

\[ Z_{\text{wind}}(T) = \frac{K(T)}{\rho(T)} \]

- Lower resistivity in the metallic bulk implies higher EM
EM on Atomic Level

- EM on atomic level is a multi-scattering process*
  - EM force exerted by scattered electrons on ions
    \[
    \vec{F} = - \int \delta n(\vec{r}) \frac{\partial V}{\partial R} d^3r
    \]
  - Electron density which depends on external field
    \[
    \delta n(\vec{r}) = \sum_k g_k |\psi_k(\vec{r})|^2
    \]
  - Shifted electron distribution
    \[
    g_k = -\frac{e\hbar \tau(k)}{m} v(k) \cdot \vec{E} \delta(\mathcal{E}_F - \mathcal{E}_k)
    \]

*Landauer, Sorbello,
Experimental observations (IMEC)
- Shorter EM lifetime with decreasing interconnect width
- Dielectric (with smaller k and Young modulus) dependence

Wen et. al. IITC 2015
New challenges: Reliability TCAD for Nanointerconnects

- Building the compact model

Compact models

- Bulk
- Schatzkes-Lloyd Parametrization
- Resistivity Model
- Electromigration Black’s equation
- Full-physical model Layout features
- Mayadas-Schatzkes Interfaces
- Fuchs-Sondheimer Grain boundaries
New challenges: Reliability TCAD for Nanointerconnects

- Simulation setting
  - Constant voltage
  - No microstructure module activated
  - Higher diffusivity on the top interface
New challenges: Reliability TCAD for Nanointerconnects

- Modifying Black’s equation

\[ t_f = t_N + t_E = \left( \frac{A(\rho)}{j^2 h^{1.6}} + \frac{B(\rho)h^2}{j} \right) \exp \left( \frac{E_a}{kT} \right) \]
Conclusion and Outlook

- Full-physics modeling provides a basis for studying general EM and related interconnect reliability problems.

- For studying particular cases it is advantageous to develop compact models relying on full-physics modeling and experiments.

- Developed compact models have been successfully applied to study reliability of multilevel interconnects, TSVs, and solder bumps.

- The multitude of reliability issues which rises with nanointerconnect technology demands an approach founded on full-physics modeling.